REMARKS

This application is a continued prosecution application (CPA) of U.S. Patent Application Serial No. 09/500,254, filed February 8, 2000. To expedite examination, Applicant has amended independent Claim 1 so as to more clearly define the claimed invention. Additionally, Applicant has provided remarks below concerning these amendments, which address various issues that were raised during prior prosecution of the application. Applicant respectfully requests entry of the amendment and examination of the application in due course.

In previous prosecution of the application, the claims have been rejected as either anticipated by U.S. Patent No. 6,321,298 to Hubis or obvious in light of the Hubis '298 patent in combination with either U.S. Patent No. 6,223,260 to Gujral et al. or U.S. Patent No. 6,021,472 to Hamaguchi.

With regard to Figure 3 of the Hubis '298 patent, a previous Office Action has alleged that the controllers **104** and the memories **202** located therein constitute shared memories. It is alleged that bus **110** acts as a copy bus, and because each controller **104** has an independent connection to the host **102**, the arrangement of the Hubis '298 patent is a shared memory anticipating the claimed invention. Applicant, however, disagrees with this assessment of the prior art.

The memories **202** of each controller **104** of the Hubis '298 patent pointed to by the previous Office Action are not shared memories, as recited in amended independent Claim 1. Specifically, a shared memory is defined in the art as a memory capable of supplying an identical database to several users, i.e., sharing the possibility of read and write accesses to identical data by all users. The memories **202** for each controller **104** of the Hubis '298 patent, on the other hand, do not supply identical databases for several users. Instead, each of these memories **202** only includes data that has been altered during processing and does not contain an entire record of all data. Specifically, as data is written to the shared storage devices **108** during processing, this written data is also stored in the memories **202** for each controller **104**. Any data located in shared memory **108** that is only read and not altered is not also stored in the memories **202** of each controller. As such, the memories **202** of each controller **104** only include data that has

been written into the shared memory, but does not include all of the data stored in the shared memory **108**. As such, each of the memories **202** of the controllers **104** does not provide an identical database to all users and are not shared memories.

Instead, the Hubis '298 patent requires the memories **202** of each controller **104** in combination with the memory devices **108** to create a shared memory. Because, the memories **202** for each controller **104** do not include a complete copy of all data and thus are not a shared memory, the controllers themselves cannot be seen as meeting the plurality of memories as recited in amended independent Claim 1. For the Hubis '298 patent to arguably meet the claimed invention, each controller **104** in combination with the shared memory **108** must be compared to amended independent Claim 1. In this instance, the system of the Hubis '298 patent does not teach or suggest the claimed invention.

The combination of each controller **104** with the shared memory **108** does not allow for internally concurrent accesses to the memory as recited in amended independent Claim 1. Specifically, the memory **108** does not have at least two access ports for concurrent access to its contents, instead only one common port is connected between the memory **108** and the controllers **104**. Specifically, as shown in Figure 3, there is only one bus **110** between the memory **108** and the controllers **104** not at least two ports, as recited in amended independent Claim 1. As such, only one controller can access the memory **108** at a time.

Further, the memory **108** is connected via the bus **110** to each of the controllers **104**. This connection is used for both copying data and for accessing data. As such, the system of the Hubis '298 patent does not teach or suggest <u>a copy bus that is independent of at least two access ports</u>, as recited in amended independent Claim 1. Instead, in the Hubis '298 system, the copy bus is also used as an access port. This is a very important distinction and accounts for a major operating difference between the memory of the claimed invention and that of the Hubis '298 patent.

Specifically, because there is only one access bus **110** connected between the controllers **104** and the memory **108**, there cannot be concurrent accesses to the memory in the Hubis '298 patent. In the Hubis '298 patent, if the host computer **102** requests data from a controller **104** that is not located in the controller's memory **202**, the controller must access the

memory **108** via the bus **112**. This action blocks all of the other controllers **104** from using the bus **112**. As such, concurrent access of the memory, as recited in amended independent Claim 1, is not possible using the system of the Hubis '298 patent.

As mentioned previously and reiterated here, the combination of the Gujral '260 and Hamaguchi '472 patents with the Hubis '296 patent does not teach or suggest a shared memory having true multi-port memories. Specifically, the Gujral '260 and Hamaguchi '472 patents do not disclose true multi-port memories. Instead, they disclose only pseudo multi-port memories. They include controllers, (which a true multi-port memory would not have), to turn concurrent reads of the two ports into sequential reads. As such, the pseudo multi-port memories support k concurrent accesses to an N port memory, while the true multi-port memory of the claimed invention provides N concurrent accesses to N ports.

In light of the above, Applicant respectfully submits that none of the cited references, taken either individually or in combination, teaches or suggests a shared memory having true multi-port memories as recited in amended independent Claim 1. As such, Applicant respectfully submits that amended independent Claim 1, as well as the claims that depend therefrom, is patentable over the cited references.

CONCLUSION

In view of the amended claims and the remarks presented above, it is respectively submitted that all of the present claims of the application are in condition for immediate allowance. It is therefore respectfully requested that a Notice of Allowance be issued. The Examiner is encouraged to contact Applicant's undersigned attorney to resolve any remaining issues in order to expedite examination of the present application.

It is not believed that extensions of time or fees for net addition of claims are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of

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this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fee required

therefore (including fees for net addition of claims) is hereby authorized to be charged to Deposit

Account No. 16-0605.

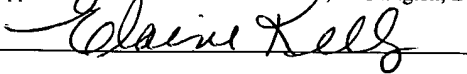<div style="text-align: right">

Respectfully submitted,

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"Express Mail" Mailing Label Number EV 034185431 US Date of Deposit: November 12, 2002 I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to Box Patent Application, Commissioner for Patents, Washington, DC 20231. _Elaine Kelly_	**CERTIFICATE OF MAILING** I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on November 11, 2002. _____ Elaine Kelly

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Version With Markings to Show Changes Made:

In the Claims:

Please amend Claim 1 as follows:

1. (Twice Amended) A shared memory comprising:

a plurality of true multi-port memories, wherein each memory has at least two access ports accessible from a user side, wherein said at least two access ports allow for internally concurrent access to data stored in the memory [having N independent ports that allow internal concurrent accesses of the memory for all N port], wherein each memory further has at least one port with a copybus-function separate from said at least two access ports [, and at least one port accessible from user side]; and

at least one copybus connected to each of said at least one ports having the copybus-function;

wherein said shared memory is adapted to copy contents of one of said multi-port memories, which has been changed by a writing operation from said user side, to other multi-port memories through said at least one copybus.

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